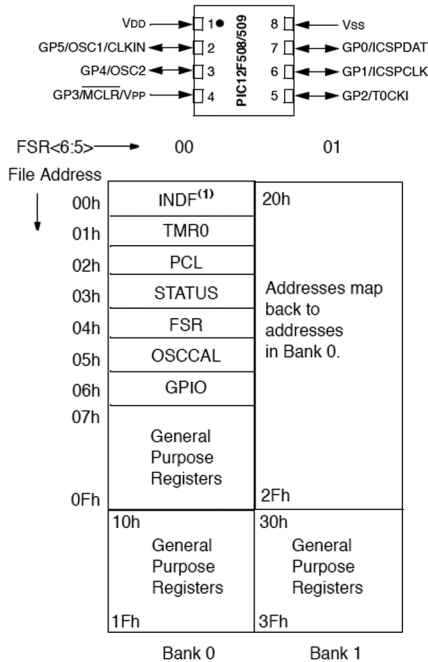




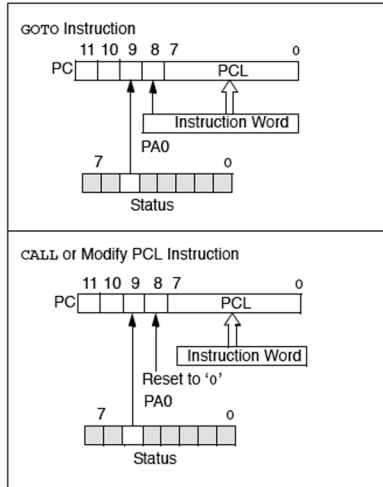
MICROCHIP

PIC12F509



Note: Because PC<8> is cleared in the CALL instruction or any modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-6: LOADING OF PC BRANCH INSTRUCTIONS



Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset ⁽²⁾	Page #
00h	INDF	Uses Contents of FSR to Address Data Memory (not a physical register)								xxxx xxxx	26
01h	TMR0	8-bit Real-Time Clock/Counter								xxxx xxxx	33
02h ⁽¹⁾	PCL	Low-order 8 bits of PC								1111 1111	25
03h	STATUS	GPWU F	—	PA0 ⁽⁵⁾	TO	PD	Z	DC	C	0-01 1xxx ⁽³⁾	20
04h	FSR	Indirect Data Memory Address Pointer								111x xxxx	26
04h ⁽⁴⁾	FSR	Indirect Data Memory Address Pointer								110x xxxx	26
05h	OSCCAL	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	1111 111-	24
06h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	29
N/A	TRISGPIO	—	—	I/O Control Register						--11 1111	29
N/A	OPTION	GPWU	GPPU	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	22

TABLE 8-2: INSTRUCTION SET SUMMARY

Mnemonic, Operands	Description	Cycles	12-Bit Opcode		Status Affected	Notes
			MSb	LSb		
ADDWF f, d	Add W and f	1	0001	11df ffff	C, DC, Z	1, 2, 4
ANDWF f, d	AND W with f	1	0001	01df ffff	Z	2, 4
CLRF f	Clear f	1	0000	011f ffff	Z	4
CLRW —	Clear W	1	0000	0100 0000	Z	
COMF f, d	Complement f	1	0010	01df ffff	Z	
DECF f, d	Decrement f	1	0000	11df ffff	Z	2, 4
DECFSZ f, d	Decrement f, Skip if 0	1 ⁽²⁾	0010	11df ffff	None	2, 4
INCF f, d	Increment f	1	0010	10df ffff	Z	2, 4
INCFSZ f, d	Increment f, Skip if 0	1 ⁽²⁾	0011	11df ffff	None	2, 4
IORWF f, d	Inclusive OR W with f	1	0001	00df ffff	Z	2, 4
MOVF f, d	Move f	1	0010	00df ffff	Z	2, 4
MOVWF f	Move W to f	1	0000	001f ffff	None	1, 4
NOP —	No Operation	1	0000	0000 0000	None	
RLF f, d	Rotate left f through Carry	1	0011	01df ffff	C	2, 4
RRF f, d	Rotate right f through Carry	1	0011	00df ffff	C	2, 4
SUBWF f, d	Subtract W from f	1	0000	10df ffff	C, DC, Z	1, 2, 4
SWAPF f, d	Swap f	1	0011	10df ffff	None	2, 4
XORWF f, d	Exclusive OR W with f	1	0001	10df ffff	Z	2, 4
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF f, b	Bit Clear f	1	0100	bbbf ffff	None	2, 4
BSF f, b	Bit Set f	1	0101	bbbf ffff	None	2, 4
BTFSC f, b	Bit Test f, Skip if Clear	1 ⁽²⁾	0110	bbbf ffff	None	
BTFSS f, b	Bit Test f, Skip if Set	1 ⁽²⁾	0111	bbbf ffff	None	
LITERAL AND CONTROL OPERATIONS						
ANDLW k	AND literal with W	1	1110	kkkk kkkk	Z	
CALL k	Call Subroutine	2	1001	kkkk kkkk	None	1
CLRWDI —	Clear Watchdog Timer	1	0000	0000 0100	TO, PD	
GOTO k	Unconditional branch	2	101k	kkkk kkkk	None	
IORLW k	Inclusive OR literal with W	1	1101	kkkk kkkk	Z	
MOVLW k	Move literal to W	1	1100	kkkk kkkk	None	
OPTION —	Load OPTION register	1	0000	0000 0010	None	
RETLW k	Return, place literal in W	2	1000	kkkk kkkk	None	
SLEEP —	Go into Standby mode	1	0000	0000 0011	TO, PD	
TRIS f	Load TRIS register	1	0000	0000 0fff	None	3
XORLW k	Exclusive OR literal to W	1	1111	kkkk kkkk	Z	

- Note 1:** The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO. See **Section 4.7 "Program Counter"**.
- 2:** When an I/O register is modified as a function of itself (e.g. MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 3:** The instruction TRIS f, where f = 6, causes the contents of the W register to be written to the tri-state latches of PORTB. A '1' forces the pin to a high-impedance state and disables the output buffers.
- 4:** If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).